

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	((signal adj interconnect)same type same language adj extension same file same partition\$3).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/13 14:31
L1	1	((signal adj interconnect) near4 type same language adj extension same file same partition\$3).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/13 14:31
S20 3	13	((FPGA PLD ) or standard adj cell) and interconnect\$3 and (\$HDL RTL) and extension adj language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 19:23
S1	15	(FPGA PLD ) same standard same interconnect\$3 same (\$HDL RTL)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 19:22
S20 2	0	717/141-144.ccls. and (rtl \$HDL) and interconnect\$3 and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 19:03
S20 1	731	717/141-144.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 18:56
S20 0	0	717/136.ccls. and (rtl \$HDL) and interconnect\$3 and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 18:52
S19 9	0	717/136.ccls. and ( PLD fpga (standard adj cell)) and interconnect\$3 and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 18:40

S19 8	0	717/136.ccls. and ( PLD fpga) and interconnect\$3 and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 18:39
S19 7	454	717/136.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 18:38
S19 6	0	716/16.ccls. and (fpga pld) and interconnect43 and (\$HDL rtl) and language adj2 extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 18:21
S19 5	553	716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 17:35
S19 4	0	716/3.ccls. and (FPGA PLD) and interconnect\$3 and (\$HDL RTL ) and (language adj extension)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 17:34
S19 2	0	716/3.ccls. and (FPGA PLD) same interconnect\$3 same (\$HDL RTL ) and language adj extension	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 17:33
S19 1	568	716/3.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/08 17:21